REMARKS

The Office Action dated September 15, 2006, has been received and carefully noted. The following remarks are being submitted as a full and complete response thereto. Claims 7-9, 14-17 and 22 are pending in this application. By this amendment, claims 7, 8 and 14 are amended, claim 6 is cancelled without prejudice to or disclaimer of the subject matter disclosed therein, and new claim 22 is added. Support for the subject matter of claim 22 can be found in the drawings at, for example, Fig. 1. No new matter has been added. Reconsideration of the rejections is respectfully requested in light of the following remarks.

The Office Action rejects claims 6-9 and 14-17 under 35 U.S.C. § 102(b)/103(a) over Miyashita et al. (U.S. Patent No. 5,951,755); and claims 6-9 and 14-17 under 35 U.S.C. § 103(a) over Wijaranakula (U.S. Patent No. 5,611,855) in view of Wolf et al. ("Silicon Processing for the VLSI Era"; Volume 1: Process Technology, Lattice Press; Sunset Beach, California, pages 26-30, 59-61, 124 and 133-136). The rejections are respectfully traversed. Claim 6 has been cancelled, and claim 22 has been added, which includes similar features to claim 6. Thus, it is assumed that the Patent Office would apply the same rejection to new claim 22.

In particular, none of the applied references, alone or in combination, disclose or suggest a manufacturing process for a silicon epitaxial wafer that includes forming new oxygen precipitation nuclei and increasing bulk defect density of the silicon substrate without reducing internal gettering by applying heat treatment to the silicon epitaxial wafer at a temperature in a range of from 450° C to 750° C, whereby the new

oxygen precipitation nuclei are uniformly formed in the substrate, as recited in independent claim 22.

Miyashita teaches a manufacturing method for manufacturing a semiconductor substrate with a first annealing step for annealing a silicon single crystal and a second annealing step for permitting oxygen embryos to contract using a second temperature range higher than the first temperature range (Abstract). Miyashita also teaches annealing a wafer in a two-step process, wherein the first step is at about 450° C to 750° C, and the second step is at about 900° C to 1100° C in order to create a non-defective layer 4 formed in a superficial layer where a device is to be made (Col. 7, lines 42-57; Figs. 1A-1C). However, Miyashita fails to disclose or suggest forming new oxygen precipitation nuclei and increasing bulk defect density, or that the new oxygen precipitation nuclei are uniformly formed in the substrate. In fact, Miyashita specifically teaches that "the interstitial oxygen concentration in the surface layer must be decreased to form a non-defective layer" (emphasis added) (Col. 2, lines 51-58; Fig. 1A-1C), and that "the invention prevents formation of BMD [bulk micro-defects] which possibly give adverse effect to device characteristics" (Col. 4, lines 62-66). Accordingly, not only Miyashita teaches away from increasing interstitial oxygen concentration in the substrate because it "give adverse effect to device characteristics," but Miyashita also fails to show that the oxygen precipitation nuclei are uniformly formed in the substrate, as is clearly from an observation of Figs. 1C and 2A. Thus, for at least these reasons, Miyashita fails to disclose, suggest or render obvious the features of independent claim 22.

Furthermore, the Patent Office is precluded from asserting that the claimed low resistivity of the silicon substrate is inherent to the teachings in Miyashita because such an assertion would imply that the low resistivity is inherent to the structures taught in Miyashita. However, MPEP §2112 states that the Patent Office must provide rationale or evidence tending to show inherency. Citing In re Robertson, 169 F.3d 743, 745, 49 USPQd 1949, 150-51 (Fed. Cir. 1990), MPEP §2112 states, "[i]nherency . . . may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient." Additionally, citing Ex Parte Levy, 17 USPQ2d 1461, 1464 (Bd. Pat. App. & Inter. 1990), §2112 states, "[i]n relying upon the theory of inherency, the Examiner must provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows from the teachings of the applied prior art" (emphasis in original). Accordingly, because there is no showing in Miyashita that a low resistivity of 0.02 Ω–cm necessarily has to flow from the taught structures, the low resistivity is not inherent from the teachings of Miyashita.

For at least these reasons, Miyashita fails to disclose, suggest or render obvious the features of independent claim 22. Thus, independent claim 22, and its dependent claims, are patentable over Miyashita.

Wijaranakula teaches a semiconductor silicon wafer used as a calibration standard for measurement of a thickness of a microdefect-free layer formed by depositing an epitaxial layer onto a substrate having an interstitial oxygen concentration suitable for precipitating oxide (Abstract).

Wolf teaches various accepted methods for silicon processing for the VLSI era. Moreover, although the Office Action admits that Wijaranakula fails to disclose or suggest the deposition temperature of the epitaxial layer, the oxygen concentration, or the substrate's resistivity (Office Action, page 5, lines 3-5), the Office Action alleges that Wolf cures deficiencies in Wijaranakula in disclosing or rendering obvious this feature. However, the Office Action is mistaken for the following two reasons.

First, Wolf merely teaches a general range of resistivity that can be used to manufacture a typical silicon wafer, but Wolf is silent on increasing the bulk defect density without reducing internal gettering, as recited in independent claim 22. Furthermore, Wijaranakula fails to disclose or suggest these properties. Wijaranakula merely teaches using an epitaxial wafer as a calibration wafer for measuring thickness of a microdefect-free layer, and teaches that the epitaxial wafer includes a bulk region having large and uniformly distributed oxide microdefects (column 3, lines 39-42). Wijaranakula further teaches that in order to reach this result, the epitaxial layer is annealed at preferably between 600° C and 900° C for preferably longer than 24 hours up to 48 hours or 72 hours (column 5, lines 33-38). In contrast, Wolf clearly teaches that in order to obtain an effective annealing step, short annealing steps "on the order of seconds at 650-750° C, have been suggested as an effective alternative annealing step" (page 61, lines 1-2). Accordingly, this teaching in Wolf, which was relied on by the Office Action (Office Action, page 5, lines 12-13), is in direct conflict with the teachings in Wijaranakula. Thus, a

combination of Wijaranakula and Wolf is improper because both references teach away from each other since Wijaranakula prefers long annealing times while Wolf prefers extremely short annealing times in the order of a few seconds. Thus, for at least this reason, the combination of Wolf and Wijaranakula does not arrive at the subject matter of independent claim 22.

Second, Wolf teaches a plurality of short cycles at 650-750° C of seconds as annealing steps (page 61, lines 1-3), and also identifies a plurality of possible annealing steps, such as the elimination of low-temperature oxygen donors at 650° C (page 60, lines 3-4), the elimination of higher temperature donors at a heat treatment at 900° C (page 60, lines 6-7), an annealing temperature at 300 to 400° C (page 60, lines 8-10) or a "normal" 1-2 hour 600-700° C annealing step to cause very small oxygen precipitates (page 60, lines 16-17). Accordingly, Wolf merely teaches a variety of possible annealing treatments, but fails to teach a step to form new oxygen precipitation nuclei, as recited in independent claim 22. Accordingly, for at least this additional reason, Wolf fails to cure deficiencies in Wijaranakula in disclosing or rendering obvious the features of independent claim 22.

For at least these reasons, independent claim 22, and its dependent claims, are patentable over all the applied references. Thus, withdrawal of the rejections of the claims under 35 U.S.C. § 102(b)/103(a) and 35 U.S.C. § 103(a) is respectfully requested.

Should the Examiner determine that any further action is necessary to place this application into better form, the Examiner is encouraged to telephone the undersigned representative at the number listed below.

In the event this paper is not considered to be timely filed, the Applicant hereby petitions for an appropriate extension of time. Any fees for such an extension, together with any additional fees that may be due with respect to this paper, may be charged to counsel's Deposit Account No. 01-2300, **referencing Attorney Dkt. No. 107242-00024**.

Respectfully submitted,

Tarik M. Nabi
Registration Number 55,478

Customer Number 004372
ARENT FOX PLLC
1050 Connecticut Avenue, NW, Suite 400
Washington, DC 20036-5339
Telephone: 202-857-6000
Fax: 202-638-4810
TMN/elz